REMARKS

In the Office Action dated June 23, 2005, the Examiner rejected claims 19, 22-24, and 26-31 under 35 USC 102(e) as "*anticipated by Nishiguchi (US Patent 5,214,308) in view of Abe et. al., (US Patent 6,288,444).*", rejected claims 20 and 25 under 35 USC 103 as unpatentable over Nishiguchi in view of Abe and further in view of Kato (US Patent 6,486,562), rejected claim 21 under USC 103 as unpatentable over Nishiguchi, Abe and Morihara (US patent 5,495,439), rejected claims 32-34 and 43 under 35 USC 103 as unpatentable over Nishiguchi, Abe and Chiu (6,391,683), rejected claims 35, 36, 37, and 39 under 35 USC 103 as unpatentable over Nishiguchi and Holzapfel (US Patent 5,872,633), rejected claim 38 under 35 USC 103 as unpatentable over Nishiguchi, Holzapfel, and Kato (US Patent 6,486,562), and rejected claims 40-42 under 35 USC 103 as unpatentable over Nishiguchi and Holzapfel. None of the claims have been amended. Claims 19-43 remain at issue.

The Art Rejection

In the June 23, 2005 Office Action, the Examiner indicated that 19, 22-24, and 26-31 were "anticipated" under 35 USC 102(e) by "Nishiguchi in view of Abe". The attorney for the applicant assumes the Examiner made an error and the rejection was intended to be a 35 USC 103(e) obviousness type rejection. The response below is made based on this assumption. The Applicants request that the Examiner confirm that this assumption is correct.

Certain claims recite that: (i) the underfill adhesive has edges that are cut around the periphery of the flip chip; and (ii) the underfill material is applied directly to the active surface of the flip chip integrated circuit.

In contrast, the Nishiguchi reference teaches the filling of the gap between a semiconductor device 1 and a substrate 3 with a bonding agent ***after*** the semiconductor device has been mounted onto the substrate. Specifically, column 3 lines 46-52 state:

> Instead of molting the bump 2, insulative bonding agent which contracts when it cures may be **filled into a gap between the semiconductor device 1 and the substrate 3** and the bump 2 may be pushed to the electrode terminal 5 by a curing contraction force of the bonding agent to electrically connect the bump 2 to the electrode terminal 5. (emphasis added)

The bonding agent at the edges of the Nishiguchi reference are therefore not: (i) cut; or (ii) applied directly to the active surface of the semiconductor device. Since the underfill material is applied to the flip chip of the present invention while in wafer form and then cut during the dicing operation, the edges of the die have clean "cut" straight vertical surfaces. In contrast, the underfill material at the edges of the Nishiguchi device would have uneven, non-straight, surfaces since the material is dispensed between the chip and the printed circuit board and then allowed to flow randomly before curing. Furthermore, the filling of the gap between the device and substrate of Nishiguchi is not the same as applying underfill adhesive directly to active surface of a flip chip.

The Abe reference is directed toward a fine pitch Ball Grid Array (BGA) package for a semiconductor chip that generates a large amount of heat during operation. The package, as best illustrated in Figure 2, includes a semiconductor chip 11 mounted within a rectangular opening located at the center of a printed wiring board 12A. See Column 4, lines 3-7. The chip 11 is in contact with a stage portion 24A of a metal heat spreader 13A. Solder balls 15 provided on the wiring board 12A, are used to mount the package onto a substrate. See column 3, lines 63-66. Wire bonds 19 are provided between the chip 11 and a wiring layer 16 of the printed wiring board 12A. See column 3, line 67 through column 4, line 2. A sealing resin 14A, made up of first and second sealing resin portions 26A and 27A, are provided on the top and bottom surfaces of the heat spreader 13A respectively. See column 5, lines 65-68.

Figure 3 of Abe illustrates a flow chart for making the package illustrated in Figure 2. After the package is fabricated as described above, it is cut along the outer periphery through the heat spreader 13, the printed wiring board 12A and the sealing resin 14A. See column 10, lines 41-46 as noted by the Examiner. The cutting step of Abe does **not** teach the cutting of the resin layer 14A around the periphery of the chip 11.

A number of important distinctions exist between the present invention and the package described by Abe: (i) the present invention is directed to a flip chip type integrated circuit package. The Abe reference is directed toward providing a heat sink for a BGA type package; (ii) solder balls are formed on the active surface of the on the flip chip of the present invention. The solder balls are used to directly mount the flip chip onto a printed circuit board substrate. In contrast, there are no solder balls formed on the chip 11 of Abe. Rather, solder balls 15 are provided on the printed wiring board 12A; (iii) the present invention defines a layer of underfill adhesive applied on the active surface of the flip chip. The underfill adhesive enhances the mounting of the flip chip to the printed circuit board substrate during reflow of the solder balls..

With the Abe reference, the is no underfill adhesive applied to the chip 11. The resin layer 14A is for protection, not for mounting the Abe package to a substrate. The resin layer 14A therefore does not enhance the bonding of the Abe package to a substrate; (iv) the present invention calls for the cutting of the edges of the underfill adhesive around the periphery of the flip chip. In contrast with Abe, there is no underfill adhesive applied to the chip 11. Furthermore, the cutting as taught by Abe occurs at the outer periphery of the printed wire board 12A, not along the peripheral sides of the chip 11.

The Examiner has failed to demonstrate a prima facie case of obviousness for a number of reasons.

The Nishiguchi and Abe references are not combinable. One is directed to the filling of the gap between a semiconductor device and a substrate with a bonding agent ***after*** the semiconductor device has been mounted onto the substrate, the other is directed to attaching a heat sink to a BGA type package. Since the Abe reference teaches the mounting of the BGA package to a printed circuit board using solder balls attached to a wire board 12A, as opposed to attaching the chip directly to a printed circuit board, the references actually teach away from one another. Accordingly, there is absolutely no teaching or suggestion in either reference that would motivate one of ordinary skill in the art to combine the references as proposed by the Examiner.

The proposed combination would also result in an inoperable device. In the Office Action, the Examiner states on page 2, the last paragraph, the following: "*Abe discloses an underfill 14, of figure 2 has cut edges at the periphery of the chip (see column 10, lines 39-46) Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to cut the bonding agent of the Nishiguchi structure at the periphery of the chip, from the surface of the substrate 3.*" In formulating the rejection, the Examiner has completely misconstrued the actual teaching of the Abe reference. The layer 14 of Abe is not an underfill or bonding layer as defined by the Examiner. It is a protective layer. As a protective layer, it presumably does not reflow and is incapable of bonding. Furthermore, it is not clear how the proposed cutting to remove excess bonding agent "*from the surface of the substrate*" could be performed without damaging or destroying the underlying substrate. The proposed combination is therefore improper.

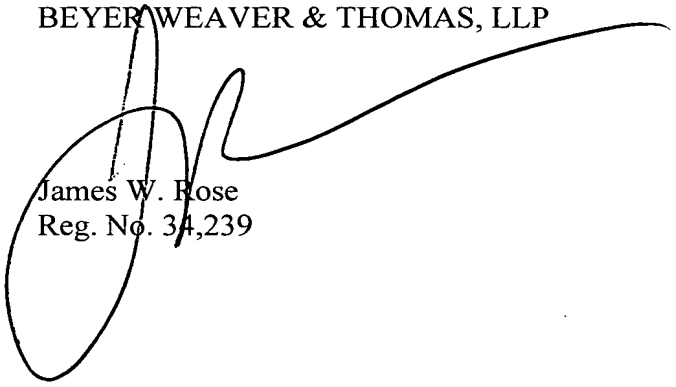
Lastly, even if it were proper to combine the two references, the proposed combination still would not result in the present invention as claimed. The proposed combination would result in either (i) the use of a bonding agent as taught by Nishiguchi to mount the BGA as taught by

Abe; or (ii) the bumped semiconductor device of Nishiguchi covered with the protective resin of Abe. Either alternative, however, still would not result in the present invention, namely a flip chip integrated circuit having an underfill adhesive layer applied on its active surface with cut edges around the periphery of the chip.

The Applicants therefore submit that pending claims are therefore patentable.

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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